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C028611(028)

B. Tech. (Sixth Semester) Examination, April-May 2022

AICTE (~~New~~ Scheme)

(Electronics & Telecommunication Branch)

VLSI DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Part (a) of each question is compulsory and it carries 4 marks. Attempt any two part from (b), (c) and (d) of each question. Part (b), (c) and (d) carry 8 marks each.*

Unit-I

1. (a) What is Transmission gate? Draw the Exclusive-OR gate using Transmission gates.

(b) Draw the CMOS schematic of 2-i/p NAND & NOR Gate and explain their operation.

(c) Design a CMOS circuit for the OAI expression

$$h = \overline{(a+b)\cdot(a+c)\cdot(b+d)}$$

Use the smallest number of transistors in your design.

(d) An inverter uses FETs with $\beta_n = 2 \cdot 1\ \text{mA/V}^2$ and $\beta_p = 1 \cdot 8\ \text{mA/V}^2$. The threshold voltages are given as $V_{Tn} = 0 \cdot 60\ \text{V}$ and $V_{Tp} = -0 \cdot 70\ \text{V}$ and the power supply has a value of $V_{DD} = 5\ \text{V}$. The parasitic FET capacitance at the output node is estimated to be $C_{FET} = 74\ \text{fF}$.

(i) Find the midpoint voltage V_M.

(ii) Find the value of R_n and R_p

(iii) Calculate the rise and fall times at the output when $C_L = 0$.

(iv) Calculate the rise and fall times when an external load of value $C_L = 115\ \text{fF}$ is connected to the output.

Unit-II

2. (a) Define Lithography.

(b) Describe the various steps involved in fabrication process of CMOS using *n*-well process.

(c) Discuss Lamda-based design rules for layout designing in brief.

(d) Draw the stick diagram and Layout for two-input CMOS NAND gate. Align the transistors horizontally.

Unit-III

3. (a) Draw the schematic of RS Flip-Flop.

(b) Design CMOS Schematic of full adder circuit using minimum number of transistors.

(c) Explain the working of 4×4 NOR-ROM and 4×4 NAND-ROM with their schematic only.

(d) Draw the Schematic of 6-T DRAM and explain the working principle.

Unit-IV

4. (a) Give the comparisons between CPLD and FPGA.

(b) (i) Consider the function $f(x_1, x_2, x_3) = \Sigma m(2, 3, 4, 6, 7)$. Show how it can be realized

using two two-input LUTs. Give the truth table implemented in each LUT. You do not need to show the wires in the FPGA.

(ii) Write the VHDL codes for 8*1 Mux using With-Select statement.

(c) Write VHDL code for Full adder using Structural Modeling styles.

(d) Write the VHDL codes for 8-line to 3-line Encoder using CASE statement.

Unit-V

5. (a) What are the differences between signals and variables?

(b) What is FSM? Differentiate Mealy and Moore FSM.

(c) Write VHDL Code for T-Flip-Flop using Behavioral modeling styles.

(d) Write the VHDL codes for Synchronous BCD counter.